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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>				Application Number	----- 10802067
				Filing Date	Herewith
				First Named Inventor	Jon M. Huppenthal et al.
				Art Unit	
				Examiner Name	
Sheet	1	of	2	Attorney Docket No.	ARB001 CON/CIP

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No. ¹	Document No. No. - Kind Code ²	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Doc	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
OC		US-6,449,170	09/2002	Nguyen et al.	
↑		US-6,051,887	04/2000	Hubbard, Robert L.	
		US-6,313,522	11/2001	Akram et al.	
		US-5,838,060	11/1998	Comer, Alan E.	
		US-6,092,174	07/18/2000	Roussakov	Entire document
		US-5,585,675	12/17/1996	Knopf	Entire document
		US-5,652,904	06/29/1997	Trimberger	Entire document
OC		US-6,072,233	06/06/2000	Corisis et al.	
		US-6,451,626	09/17/2002	Lin	
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FOREIGN PATENT DOCUMENTS							
Examiner Initials	Cite No. ¹	Foreign Patent Document		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Doc	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear	T ⁶
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NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s) publisher, city and/or country where published	T ²
DC		HINTZKE, JEFF, Probing Thin Wafers Requires Dedicated Measures, http://www.eleetroglas.com/products/White%20Paper/Hintzke Thin Paper.html , Electroglas, Inc. Aug. 21, 2001, pp. 1-6.	
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		System Architecture, http://www.srccomp.com/products.htm , SRC Computers, Inc., Aug. 22, 2001, pp.1-2.	
		Configurations, SRC Expandable Node, http://www.srccomp.com/products_configs.htm , SRC Computers, Inc. Aug. 22, 2001, p.1.	
		YOUNG, JEDEDIAH J., MALSHE, AJAY P., BROWN, W.D., LENIHAN, TIMOTHY, ALBERT, DOUGLAS, OZGUZ, VOLKAN, Thermal Modeling and Mechanical Analysis of Very Thin Silicon Chips for Conformal Electronic Systems, University of Arkansas, Fayetteville, AR, pp.1-8, 2001 <i>Nonconformal</i>	
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		SAVASTIOUK, SERGEY, SINIAGUINE, OLEG, FRANCIS, DAVID, Thinning Wafers for Flip Chip Applications, http://www.iii1.com/hdi/article.html , International Interconnection Intelligence, Oct. 18, 2001, pp. 1-13.	
		SAVASTIOUK, SERGEY, SINIAGUINE, OLEG, KORCZYNSKI, ED, Ultra-thin Bumped and Stacked WLP using Thru-Silicon Vias, http://www.ectc.net/advance_program/abstracts2000/s15p1.html , Tru-Si Technologies, Inc., Oct. 18, 2001, p. 1.	
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↓		SAVASTIOUK, SERGEY, Moore's Law- the z dimension, http://www.trusi.com/article7.htm , SolidState Technology, Oct. 18, 2001, pp. 1-2.	
DC		Through-Silicon Vias, http://www.trusi.com/throughsiliconvias.html , Tru-Si Technologies, Oct. 18, 2001, p. 1.	

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